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Mail Stop Certificate of Corrections Branch Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

Re:

U.S. Patent No.: 6,791,085 B2

Issued: September 14, 2004 Inventor: Jean-Luc Martin et al.

Our Docket: 34149

Certificate
0CT 1 5 2004

of Correction

Sir:

A Certificate of Correction under 35 U.S.C. 254 is hereby requested to correct Patent Office printing errors in the above-identified patent. Enclosed herewith is a proposed Certificate of Correction (Form No. PTO-1050) for consideration along with appropriate documentation supporting the request for correction.

It is requested that the Certificate of Correction be completed and mailed at an early date to the undersigned attorney of record. The proposed corrections are obvious ones and do not in any way change the sense of the application.

We understand that a check is not required since the errors were on the part of the Patent and Trademark Office in printing the patent.

Very truly yours,

1 8 OCT 2004

JJS:vln Enclosures I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date indicated below.

Jeffrey J. Sopko

Name of Attorney for Applicant(s)

October 5, 2004

Date

Signature of Attorney

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO.

: 6,791,085 B2

PAGE 1 OF 1

DATED

: September 14, 2004

INVENTOR(S)

: Jean-Luc Martin et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 6

Line 32, please delete " I_{eb2} " and insert therefor - - I_{eb1} - -.

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PATENT NO. <u>6,791,085 B2</u>

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previously stored in an external memory and calculated specifically for each micro-bolometer 2.

Figure 4 shows a second embodiment in which the second thresholding branch 30 comprises only a second transistor 36 controlled directly by a generator 50 able to deliver a DC analogue voltage. This voltage is applied to the second transistor 36 to regulate the current $I_{\rm eb2}$.

As in the first embodiment, the current I_{eb2} in the second branch 30 is calculated in such a way that the dynamic of the current I_{mes} is located in the dynamic of the read module 8 input stage.

Figure 5 shows a third embodiment of the invention in which the second branch 30 comprises three subbranches 52, 54 and 56 mounted in parallel, each subbranch being able to conduct a pre-set current. The value of the current in each of the sub-branches 52, 54 and 56 is fixed by a transistor 57, 58 and 59 respectively in saturation regime provided in series with the corresponding sub-branch. A saturation regime transistor being an electrical equivalent to a current source.

The principle still consists in subtracting a thresholding current in at least two branches. The first branch makes it possible to subtract a constant current I_{eb1} and the second branch makes it possible to subtract a current I_{eb2} adapted to each detector and calculated as a function, on the one hand of its specific bolometric resistance, and on the other hand of the temperature of the focal plane. Each sub-branch 52, 54 and 56 allows a different current to be extracted representing a fraction

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